HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, Colorado 80527-2400

PATENT APPLICATION

ATTORNEY DOCKET NO. 200301840-2

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David H. ASHER et al. **Confirmation No.:**

Application No.: Unassigned **Examiner:**

Filing Date: Herewith **Group Art Unit:**

Title: METHOD AND SYSTEM FOR ABSORBING DEFECTS IN HIGH PERFORMANCE MICROPROCESSOR WITH A LARGE N-WAY SET ASSOCIATIVE CACHE

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

This Information Disclosure Statement is submitted:

(X) under 37 CFR 1.97(b), or
(Within three months of filing national application; or date of entry of national application; or before mailing date of first office action on the merits; whichever occurs last)

( ) under 37 CFR 1.97(c) together with either a:
( ) Statement under 37 CFR 1.97(e), or
( ) a $180.00 fee under 37 CFR 1.17(p), or
(After the CFR 1.97 (b) time period, but before final action or notice of allowance, whichever occurs first)

( ) under 37 CFR 1.97 (d) together with a:
( ) Statement under 37 CFR 1.97(e)(1) or (2), and
( ) a $180.00 fee set forth in 37 CFR 1.17(p).
(Filed after final action, a notice of allowance, on or before payment of the issue fee)

Please charge to Deposit Account **08-2025** the sum of $0.00 . At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account **08-2025** pursuant to 37 CFR 1.25.

(X) Applicant(s) submit herewith Form PTO 1449 - Information Disclosure Statement together with any required copies of patents, publications or other information of which applicant(s) are aware, which applicant(s) believe(s) may be material to the examination of this application and for which there may be a duty to disclose in accordance with 37 CFR 1.56.

( ) A concise explanation of the relevance of foreign language patents, foreign language publications and other foreign language information listed on PTO Form 1449, as presently understood by the individuals(s) designated in 37 CFR 1.56 (c) most knowledgeable about the content is given on the attached sheet, or where a foreign language patent is cited in a search report or other action by a foreign patent office in a counterpart foreign application, an English language version of the search report or action which indicates the degree of relevance found by the foreign office is listed on form PTO 1449 and is enclosed herewith.

It is requested that the information disclosed herein be made of record in this application.

"Express Mail" label no. **EV303486151US**

Date of Deposit **10/21/2003**

I hereby certify that this is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to: Commissioner for Patents, Alexandria, VA 22313-1450.

By Colleen F. Brown

Typed Name: **Colleen F. Brown**

Respectfully submitted,

David H. ASHER et al.

By _____

Dani I J. Krueger

Attorney/Agent for Applicant(s)
Reg. No. **42,771**

Date: **10/21/2003**

Telephone No.: **(713) 238-8055**

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))	ATTY.DOCKET NO. 200301840-2 (1662-29501)	SERIAL NO. Unassigned
	APPLICANTS David H. ASHER et al.	
	FILING DATE Herewith	GROUP

U. S. PATENT DOCUMENTS

Examiner Initial		Patent Number							Issue Date	Patentee	Class	Sub-class	Filing Date (If Appropriate)
	AA	5	2	6	1	0	6	6	11/09/93	Jouppi et al.	395	425	03/27/90
	AB	5	3	1	7	7	1	8	05/31/94	Jouppi	395	425	01/25/93
	AC	5	7	5	8	1	8	3	05/26/98	Scales	395	825	07/17/96
	AD	5	7	6	1	7	2	9	06/02/98	Scales	711	148	07/17/96
	AE	5	7	8	7	4	8	0	07/28/98	Scales et al.	711	148	07/17/96
	AF	5	8	0	2	5	8	5	09/01/98	Scales et al.	711	154	07/17/96
	AG	5	8	0	9	4	5	0	09/15/98	Chrysos et al.	702	186	11/26/97
	AH	5	8	7	5	1	5	1	02/23/99	Mick	365	233	05/28/97
	AI	5	8	9	0	2	0	1	03/30/99	McLellan et al.	711	108	07/01/97
	AJ	5	8	9	3	9	3	1	04/13/99	Peng et al.	711	206	01/15/97
	AK	5	9	1	8	2	5	0	06/29/99	Hammond	711	205	05/05/95
	AL	5	9	1	8	2	5	1	06/29/99	Yamada et al.	711	207	12/23/96
	AM	5	9	2	3	8	7	2	07/13/99	Chrysos et al.	395	591	11/26/97
	AN	5	9	5	0	2	2	8	09/07/99	Scales et al.	711	148	02/03/97
	AO	5	9	6	4	8	6	7	10/12/99	Anderson et al.	712	219	11/26/97
	AP	5	9	8	3	3	2	5	11/09/99	Lewchuk	711	137	12/09/97
	AO	6	0	0	0	0	4	4	12/07/99	Chrysos et al.	714	47	11/26/97
	AR	6	0	7	0	2	2	7	05/30/2000	Rokicki	711	117	10/31/97
	AS	6	0	8	5	3	0	0	07/04/2000	Sunaga et al.	711	168	09/19/97
	AT	6	0	5	5	2	0	4	04/25/2000	Bosshart	365	230.06	04/28/98
	AU	6	3	5	1	7	9	7	02/26/2002	Beard et al.	711	207	11/13/98
	AV	5	6	6	6	4	8	2	09/1997	McClure	714	8	
	AW	5	0	7	0	5	0	2	12/1991	Supnik	714	8	
	AX	5	9	5	3	7	4	5	09/1999	Lattimore et al.	711	162	
	AY	5	9	5	8	0	6	8	09/1999	Arimilli et al.	714	8	

FORM PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary) (37 CFR 1.98(b))	ATTY. DOCKET NO. 1662-29500 (P00-3182)	SERIAL NO. 09/651,948
	APPLICANTS David H. ASHER et al.	
	FILING DATE August 31, 2000	GROUP 2185

OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication)			
		AZ	*Alpha Architecture Reference Manual*, Third Edition, The Alpha Architecture Committee, 1998 Digital Equipment Corporation (21 p.), in particular pages 3-1 through 3-15
		BA	*A Logic Design Structure For LSI Testability*, E. B. Eichelberger et al., 1977 IEEE (Pages 462-468)
		BB	*Direct RDRAM™256/288-Mbit (512Kx16/18x32s)*, Preliminary Information Document DL0060 Version 1.01 (69 p.)
		BC	*Testability Features of AMD-K6™Microprocessor*, R. S. Fetherston et al., Advanced Micro Devices (8 p.)
		BD	*Hardware Fault Containment in Scalable Shared-Memory Multiprocessors*, D. Teodosiu et al., Computer Systems Laboratory, Stanford University (12 p.), 1977
		BE	*Cellular Disco: resource management using virtual clusters on shared-memory multiprocessors*, K. Govil et al., 1999 ACM 1-58113-140-2/99/0012 (16 p.)
		BF	*Are Your PLDs Metastable?*, Cypress Semiconductor Corporation, March 6, 1997 (19 p.)
		BG	*Rambus® RIMM™Module (with 128/144Mb RDRAMs)*, Preliminary Information, Document DL0084 Version 1.1 (12 p.)
		BH	*Direct Rambus™RIMM™Module Specification Version 1.0*, Rambus Inc., SL-0006-100 (32 p.), 2000
		BI	*End-To-End Fault Containment In Scalable Shared-Memory Multiprocessors*, D. Teodosiu, July 2000 (148 p.)
Examiner			Date Considered
EXAMINER: Initial citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			